

## CLAIMS

1. A receiving device for carrying out an interpolating synchronous detection when receiving a code division multiple signal, comprising:

5 storage means for storing receive data which are an object to be detected synchronously; and

control means for switching a storage of the receive data which are the object to be detected synchronously in the storage means before or after a reverse diffusion.

10 2. The receiving device according to claim 1, wherein the control means changes a storage order for the receive data based on symbol rate information obtained when demodulating the receive data.

15 3. The receiving device according to claim 1, wherein the control means changes a storage order for the receive data based on multipass information obtained when demodulating the receive data.

20 4. The receiving device according to claim 1, wherein the control means changes a storage order for the receive data in response to an instruction sent from a power control system of the receiving device.

25 5. The receiving device according to any of claims 1 to 4, further comprising means for carrying out a receipt processing corresponding to a plurality of multipasses, thereby rake synthesizing a plurality of receiving signals demodulated on a pass correspondence.

6. The receiving device according to any of claims 1 to 5, further comprising means for independently receiving a pilot symbol to carry out a

phase estimation for a synchronous detection and receiving a data symbol, the control means carrying out a switching control for a storage of the received data symbol which are the object to be detected synchronously in the storage means before or after the reverse diffusion when independently receiving the pilot  
5 symbol and the data symbol respectively.

7. The receiving device according to any of claims 1 to 6, wherein a reverse diffusion processing and a synchronous detection processing for receiving signals of a plurality of channels are carried out by using an identical  
10 circuit.

8. The receiving device according to any of claims 1 to 7, wherein a reverse diffusion processing and a synchronous detection processing for receiving signals of a plurality of passes are carried out by using an identical  
15 circuit.

9. The receiving device according to any of claims 1 to 8, wherein a reverse diffusion processing, a synchronous detection processing and a rake synthesis processing for a plurality of passes and a plurality of channels are  
20 carried out at the same time by using an identical circuit.

10. The receiving device according to any of claims 1 to 9, wherein the storage means has storage memories corresponding to an oversampling degree or a plurality of storage memories.  
25

11. The receiving device according to any of claims 1 to 8, wherein receive data read continuously from the storage means are consecutively diffused reversely.

12. The receiving device according to any of claims 1 to 11, wherein receive data read from the storage means in an optional order are diffused reversely.

13. The receiving device according to any of claims 1 to 12, wherein the control means changes contents of a calculation in accordance with a program.

14. The receiving device according to any of claims 1 to 13, wherein the storage means divides the data obtained before and after the reverse diffusion and stores them therein, respectively.

15. The receiving device according to claim 14, wherein the control means changes a storage order for the receive data depending on a symbol rate and the number of fingers in each of a plurality of receiving channels.

16. The receiving device according to claim 14, wherein when an error is found in a demodulating signal of a receiving signal, data stored in the storage means are synthesized with data retransmitted in accordance with a hybrid ARQ method.

17. A semiconductor integrated circuit comprising the receiving device according to any of claims 1 to 16.

18. A communicating device comprising the receiving device according to any of claims 1 to 16 or the semiconductor integrated circuit according to claim 17, wherein a code division multiplex communication is carried out.